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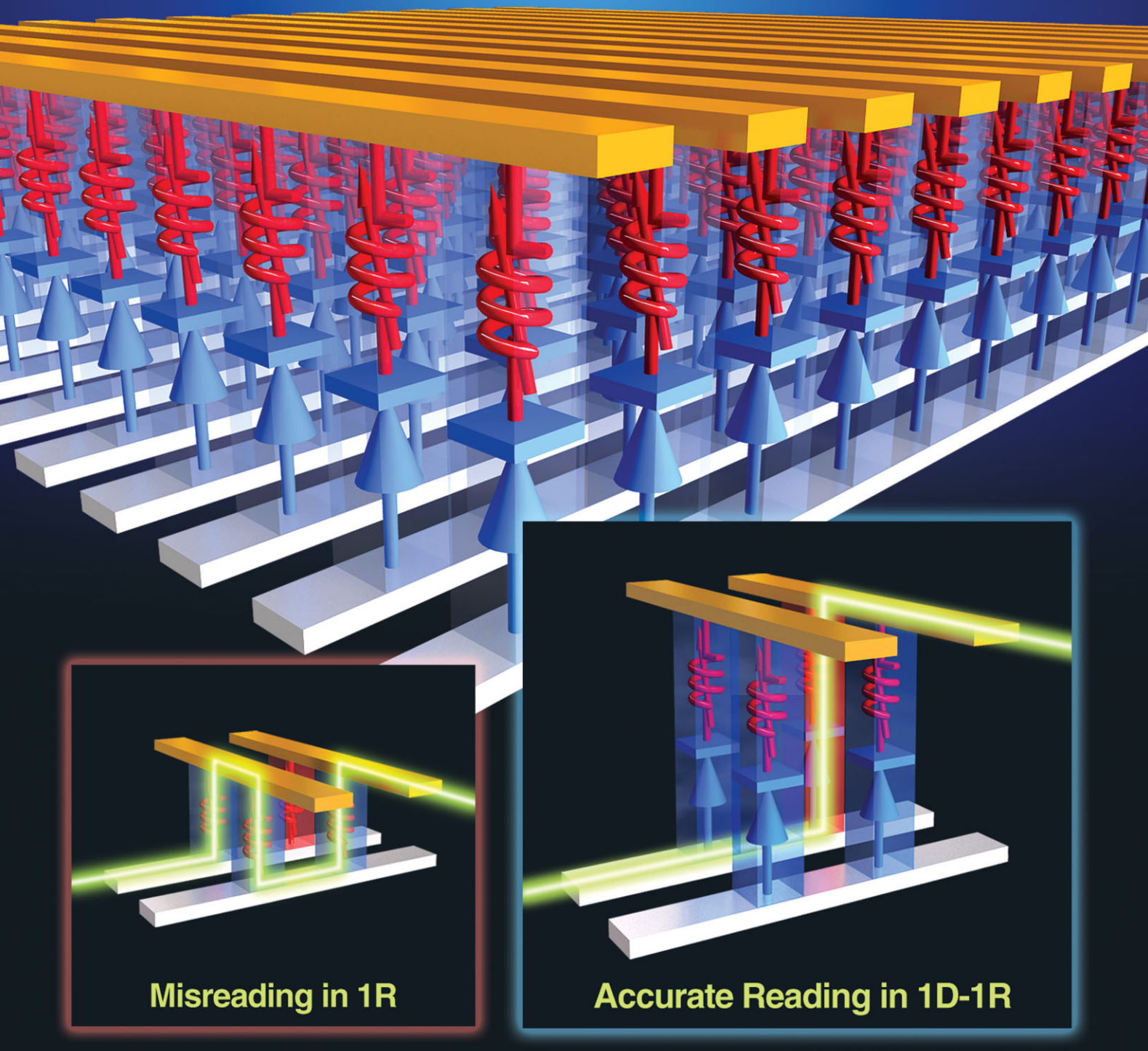

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Organic Memory

COMMUNICATION

Rewritable Switching of One Diode–One Resistor Nonvolatile Organic Memory Devices

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Recently, organic electronics including organic light-emitting diodes, transistors, and solar cells have attracted considerable attention due to a variety of advantages such as printability, flexibility, low processing cost, and easy fabrication.[1–4] In particular, with the miniaturization of electronic devices and the exponential growth of information technologies, since organic resistive memories were first introduced by Yang and coworkers they have been extensively investigated as a promising alternative to conventional semiconductor-based nonvolatile memory.[5–15] However, research interests have only focused on developing new organic materials or optimizing device structures.[11–15] The essential step for practical application of the organic memories should be accurately sensing resistance states of individual memory cells in array-type integrated circuit.

Cross-talk interference between memory cells can occur due to leakage current paths (called sneak paths) through neighboring cells with low resistances in cross-point array structures[16,17] or an excess of current that may induce electrical damage.[18] This phenomenon disturbs the reading process of the selected cell, which must be absolutely eliminated to enable practical memory applications. The indicated solution to eliminate this cross-talk is adding a rectifying diode to each cell.[19] The International Technology Roadmap for Semiconductors (ITRS) also suggested that the combination of a diode or transistor with a resistor in a single chip is indispensable for the prevention of this undesired cross-talk.[20] The architecture of one diode and one resistor (1D–1R)[6,16,17,21–24] or one transistor and one resistor (1T–1R)[18,25] can improve reading accessibility in an integrated memory array structure. Recently, we reported 1T–1R hybrid-type devices consisting of a silicon transistor and a resistive organic memory, where the operation of 1T–1R could be controlled by the resistance state of the organic memory.[25] The 1D–1R architecture is preferred in terms of integration because it occupies less area ($4F^2$, where F is a minimum feature size). Furthermore, the design and fabrication of 1D–1R devices are simpler than for 1T–1R devices. The use of an unpatterned storage medium consisting of a phase-separated blend of an organic ferroelectric and a semiconducting polymer did yield bistable rectifying diodes,[26] which has been suggested as the ultimate solution of the cross-talk problem in organic memories. Recently, a write-once read-many (WORM) memory with a diode[22] or diode-switch organic nonvolatile bistable memory (DS-ONBM)[23] was demonstrated. However, the electrically irreversible switching of these devices limits their practical applications that often require a rewritable capability. Electrically rewritable cells in the 1D–1R structure can be achieved only by the introduction of unipolar-type switching as memory elements that can be set and reset at the same voltage polarity.[16,17,24] In addition, as compared with a Si-based diode, poor performance and poor reliability of organic-based diode switches have been obstacles to reliable operation of the 1D–1R system. Therefore, a hybrid-type 1D–1R structure combining an inorganic diode and an organic unipolar memory may be preferred.

In this work, we report on the development of 1D–1R hybrid-type devices consisting of inorganic Schottky diodes and organic unipolar memory, demonstrating electrically rewritable switching in the 1D–1R system. The 1D–1R array architecture improves the sensing efficiency of the array memory cell, ultimately creating the possibility for high-density integrated organic memory devices without restrictions due to cross-talk between cells.

Figure 1a illustrates a schematic of the 1D–1R devices with 16 unit cells (see Figure S1 in the Supporting Information for an optical image of the 1D–1R devices). The schematic layer structure and electronic circuit diagram of the devices are shown in Figure 1b. In the 1D–1R devices, the diode component is an inorganic Schottky diode made from Al and p-type Si and the resistive memory component is made of a composite material of polyimide (PI) and 6,6-phenyl-C61 butyric acid methyl ester (PCBM) (denoted PI:PCBM). Figure 1c shows a transmission electron microscopy (TEM) image of an inorganic Schottky junction. Figure 1d presents a TEM image of the organic memory, demonstrating the memory cell with stacked Al/PI:PCBM/Au layers. No PCBM aggregates were observed in Figure 1d, indicating homogenously dispersed PCBM molecules in the PI matrix. TEM energy dispersive X-ray spectroscopy (EDX) analysis confirms that the switching effect is not due to filamentary paths created by unintentional penetration of Au metal into the

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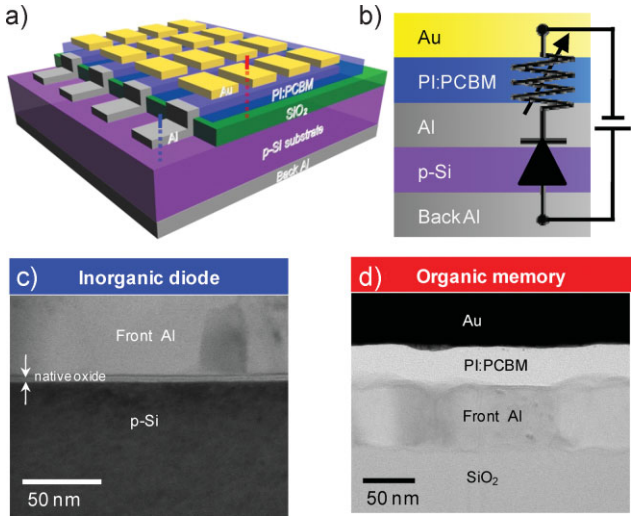


Figure 1. a) A schematic of 1D–1R hybrid-type memory devices. Blue and red lines indicate the inorganic Schottky diode (1D) component and the organic resistive memory (1R) component, respectively. b) A schematic of the layered structure and an electronic circuit diagram of the 1D–1R device. c) A TEM image of an inorganic Schottky junction diode (across the blue line in (a)). d) A TEM image of the organic memory (Al/PI:PCBM:Au) (across the red line in (a)).

PI:PCBM composite film (see Figure S3 in the Supporting Information).

The current–voltage (I–V) characteristics of a unit cell of the inorganic Schottky diode and the organic resistive memory were tested. Figure 2a shows the I–V characteristics of the Schottky diode with its circuit diagram (left inset). The metal–semiconductor junction (Al/p-Si) exhibited nonlinear diode characteristics, as shown in Figure 2a. In the voltage range of –10 to 10 V, the current level in forward bias conditions (i.e., when a positive voltage was applied to p-Si) was much higher than that in reverse bias conditions (i.e., when a negative voltage was applied to p-Si), demonstrating typical rectification properties. The Schottky diode presented excellent rectifying properties with a high rectification ratio, for example, approximately 10^4 at $\pm$2.3 V, as shown in the right inset of Figure 2a.

Figure 2b shows the typical unipolar memory switching behavior and its circuit diagram. There are two types of switching behaviors in nonvolatile organic memory devices: unipolar switching and bipolar switching. Unipolar switching is achieved by successive application of voltages with the same polarity,[27] whereas bipolar switching requires both positive and negative voltages for the writing or erasing process.[28,29] A 1D–1R device with bipolar memory cannot operate properly because it is not erasable due to the suppressed current at the reverse polarity. Therefore, unipolar memory is required for proper operation of 1D–1R devices. As shown in Figure 2b, by sweeping the voltage from 0 to 4 V and then back from 4 to 0 V, the device was switched from an initial high resistance state (OFF) to a low resistance state (ON) at the threshold voltage ($V_{th} \approx 2.8$ V) (first curve in Fig. 2b). When the voltage was ramped up again from 0 to 8 V, the device remained in the low resistance state (ON). Then, there was a local current maximum ($V_{max} \approx 3.3$ V) followed by a negative differential resistance (NDR) region and a local current minimum ($V_{min} \approx 5.9$ V) (second curve). From these results, the operating voltages of organic memory for writing, erasing, and reading were determined to be ~4, 8, and 1 V, respectively. Note these operating voltage conditions could be similarly applied in the negative voltage regimen (third and fourth curves). In particular, any voltage in the NDR region can set an intermediate state between the ON and OFF states, providing the possibility of multibit memory (see Figure S4 in the Supporting Information). The PI:PCBM composite material was previously reported to be a potential active medium for organic memory with thermal robustness as well as multilevel programming capabilities.[30] The resistive switching phenomenon is associated with the charge-trapping mechanism described by Simmons and Verderver[31] and Bozano et al.[32,33]

Figure 2c shows the I–V characteristics of a combined 1D–1R memory cell (p-Si/Al/PI:PCBM/Au). These characteristics clearly show that the memory and diode functions work together. Reversible switching characteristics of the unipolar memory were observed in forward bias conditions, while the switching in reverse bias conditions was significantly suppressed due to the

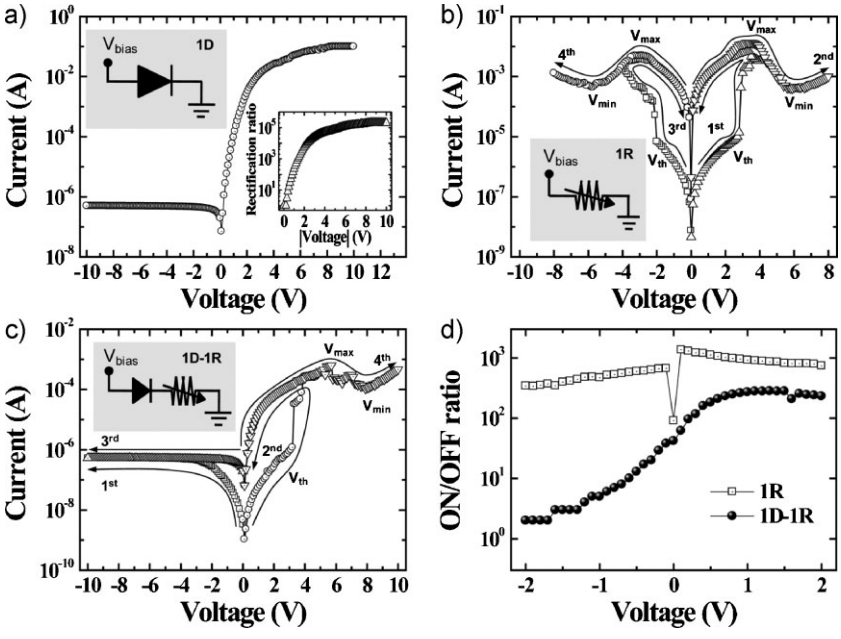


Figure 2. a) I–V characteristics and circuit diagram (left inset) of an inorganic Schottky diode. The right inset shows the rectification ratio as a function of voltage. b) I–V characteristics of an organic resistive memory and its circuit diagram (inset). V_{th}, V_{max}, and V_{min} indicate the threshold voltage, the voltage at the local current maximum point, and the voltage at the local current minimum point, respectively. c) I–V characteristics and circuit diagram (inset) of a 1D–1R memory device. d) Comparison of the ON/OFF ratios for 1R and 1D–1R devices as a function of the applied voltage.

rectifying property of the diode. Specifically, no considerable current flow occurred during the reverse voltage sweep (first curve in Fig. 2c), while the current increased sharply at the threshold voltage ($V_{th} \approx 3.2$ V) in the forward voltage sweep (second curve), indicating a switch from the OFF to ON state. The current track in the subsequent reverse sweep (third curve) was nearly identical to the rectifying current of the diode device alone (Fig. 2a). The 1D–1R devices were erased by a forward voltage sweep (fourth curve), resulting in an N-shaped *I*–*V* curve (i.e., a local current maximum ($V_{max} \approx 5.7$ V) followed by NDR and a local current minimum ($V_{min} \approx 8$ V). To evaluate the rectifying properties of memory devices connected with the diode component, ON/OFF ratios for 1R (resistive memory devices only) and 1D–1R devices as a function of the applied voltage were compared (Fig. 2d). The ON/OFF ratio of the resistive memory (1R) had nearly the same value regardless of the voltage polarity. This is due to the symmetrical *I*–*V* behavior of the 1R (Fig. 2b). However, the ON/OFF ratios of 1D–1R devices were significantly different depending on the voltage polarity. This is due to current suppression by the diode device component for the reverse voltage.

It is important to investigate the device-to-device uniformity of organic memory devices. A statistical analysis of switching characteristics of a set of 35 unit cells was performed for both 1R and 1D–1R memory devices. Figure 3a shows the cumulative probability data for each resistance state of the devices. Regardless of the type of device, both the ON and OFF resistances exhibited a narrow distribution (1–2 orders of magnitude) with a good separation between the ON and OFF states. In particular, the average resistance (~50 kΩ) of the ON state in the 1D–1R devices was 50 times higher than that (~1 kΩ) of the 1R devices. This difference is attributed to the increased series resistance of the added diode component. These results suggest that the forward resistance of the diode component affects the ON/OFF ratio in the 1D–1R devices, especially by changing the ON current level. In contrast, the OFF resistances of the 1D–1R devices were nearly the same as those of the 1R devices, indicating that the OFF resistances are primarily governed by the insulating properties of the organic film.

We also investigated the threshold voltage distributions extracted from *I*–*V* plots of each set of 35 unit cells for both 1R and 1D–1R devices (Fig. 3b). The threshold voltages of the 1D–1R devices were higher than those of the 1R devices. This is likely due to the voltage sharing of the series-connected devices (the diode and memory components). The performance of both the 1R and 1D–1R devices was evaluated and compared in terms of endurance and retention. The endurance cycling test was performed by repetitive sweeping operations of a single cell (Fig. 3c). During 280 sweep cycles, both 1R and 1D–1R devices kept two stable current states without any significant electrical degradation. In addition, the devices showed good rewritable characteristics during write–read–erase–read cycling test performed by repeating voltage pulses (see Figure S6 in the Supporting Information). To evaluate the ability to retain information, retention times of the devices were characterized and are shown in Figure 3d. Both 1R and 1D–1R devices presented good retention characteristics (10^4 s) with extrapolated retention times of more than 1 year. Note that the actual lifetime of the devices can be much longer than 10^4 s, indicating a reasonably stable behavior in terms of information storage capability.

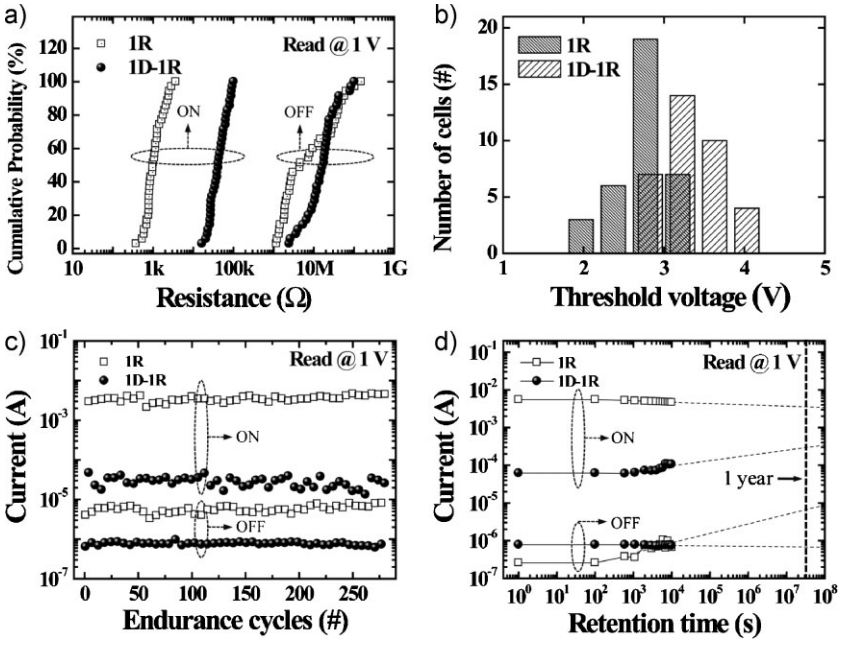
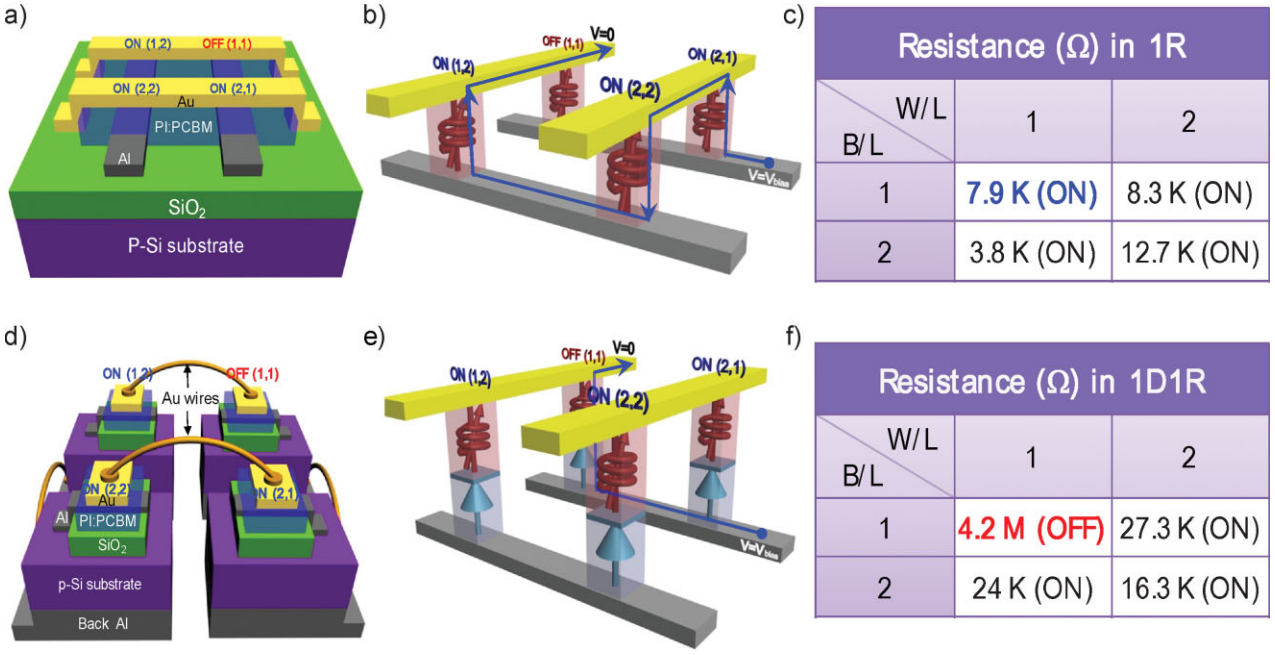


Figure 3. a) Cumulative probability data of each ON and OFF resistance for 1R and 1D–1R devices. ON and OFF resistances were measured at a voltage of 1 V. b) Comparison of the threshold voltage distributions of 1R and 1D–1R devices. c) Endurance cycles of 1R and 1D–1R devices. d) Retention times of 1R and 1D–1R devices. The extrapolated retention time can be estimated as more than 1 year.

The essence of 1D–1R devices is controlling the ON and OFF states of each cell in array-type circuit devices. For example, in integrated cross-point array-type memory devices, parasitic paths can exist in parallel to the selected cell through the neighboring cells if the polymers lack current-rectification properties.[16,17] These paths can affect the reading process, causing misreading errors (i.e., cross-talk phenomena). We experimentally observed such interference problems occurring between memory cells in 1R cross-point array-type memory devices (Fig. 4a–c) (see Figure S7 in the Supporting Information for an optical image of 1R array-type devices). Specifically, when (1,2), (2,1), and (2,2) cells were set to ON states and the (1,1) cell was initially set to the OFF state, the (1,1) cell would appear to be in the ON resistance (7.9 kΩ) due to leakage path ((2,1) → (2,2) → (1,2)) through neighboring ON cells. This indicates that any OFF state of a memory cell can be misread as an ON signal in 1R array devices. This cross-talk problem can be solved by employing diodes in the 1D–1R array memory architecture. If rectifying diode components are integrated into the resistive memory cells, the current path through the (2,2) cell can be broken with a proper diode



Resistance (Ω) in 1R		
W/L / B/L	1	2
1	7.9 K (ON)	8.3 K (ON)
2	3.8 K (ON)	12.7 K (ON)

Resistance (Ω) in 1D1R		
W/L / B/L	1	2
1	4.2 M (OFF)	27.3 K (ON)
2	24 K (ON)	16.3 K (ON)

Figure 4. a–c) The reading process of the 1R array-type memory device. a) Schematic of the 1R device with 2 × 2 cells. b) Schematic illustrating the cross-talk interference during reading of an OFF (1,1) cell when neighboring cells ((1,2), (2,1), and (2,2)) were set to the ON state. c) Resistance values of each cell in the 1R device. Each resistance was measured at a voltage of 1 V. The (1,1) cell was misread as an ON signal due to interference from neighboring cells during reading. d–f) The reading process of the 1D–1R array-type memory device. d) Schematic of the 1D–1R device, which is made of four 1D–1R unit cells that are connected by Au wires. e) Schematic illustrating current flow during reading of an OFF (1,1) cell when neighboring cells ((1,2), (2,1), and (2,2)) were set to the ON state. f) Resistance values of each cell in the 1D–1R device. Each resistance was measured at a voltage of 1 V. The (1,1) cell was accurately read as an OFF signal, demonstrating the absence of the cross-talk problem.

component and misreading can be avoided. To this end, we developed an array device with 2 × 2 matrix cells that consist of 1D–1R unit cells connected with Au wires, as shown in Figure 4d. As illustrated in Figure 4e and f, even when ON states were formed in neighboring cells (i.e., the (1,2), (2,1), and (2,2) cells), the OFF signal of the selected (1,1) cell was successfully maintained without any electrical interference from neighboring cells, showing the desired high resistance of 4.2 MΩ (OFF state). Accurate cell readings were possible in the 1D–1R array-type devices because the diode components integrated with the memory components suppressed the reverse current flow from top electrodes toward bottom electrodes.

In conclusion, this work demonstrates the successful development of 1D–1R hybrid-type devices consisting of an inorganic Schottky diode and organic unipolar memory components. The 1D–1R memory devices have electrically rewritable switching characteristics as well as rectifying properties. We constructed array-type 1D–1R memory devices in which cross-talk reading interference was successfully prevented. This enhanced reading capability will enable the development of high-density integrated nonvolatile organic memory for a variety of applications.

Experimental

Inorganic Schottky diodes were fabricated on a p-type (100) silicon substrate with a resistivity of 8–12 Ω · cm. After a typical ultrasonic cleaning process, SiO_2 (with a thickness of 2000 Å) was deposited onto the p-Si substrate using plasma-enhanced chemical vapor deposition (PECVD). The SiO_2 was then patterned by photolithography and submitted to an etching process with buffered oxide etchant (BOE). To make an ohmic back-contact of the diode, 1000-Å-thick Al was deposited onto the back side of the p-Si substrate using an electron-beam evaporator at a pressure of $\sim 10^{-7}$ Torr and submitted to thermal annealing at 550 °C under an Ar atmosphere for 20 min. Schottky junctions were formed on the front side of the p-Si substrate by evaporating the Al. Al was also used to make the bottom electrodes of the organic resistive memory component. The junction area of the Schottky diode was 1 mm × 1 mm.

To make an active layer of organic resistive memory, biphenyltetracarboxylic acid dianhydride p-phenylene diamine (BPDA-PPD), used as a PI precursor, was dissolved in *N*-methyl-2-pyrrolidone (NMP) solvent (BPDA-PPD:NMP = 1:3 by weight). PCBM was also dissolved in NMP solvent at a concentration of 0.5 wt%. A PI:PCBM composite solution was then prepared by mixing the PI solution (2 mL) with the PCBM solution (0.5 mL). The Al surface on the p-Si substrate was exposed to UV-ozone treatment for 10 min to improve reliability of organic resistive memory.[34] The PI:PCBM composite solution was then spin-coated onto the substrate at 2000 rpm for 40 s. The coated film was soft baked at 120 °C on a hotplate for 10 min to evaporate the solvent and then submitted to a thermal curing process at 300 °C under a nitrogen atmosphere for 30 min. The thickness of the PI:PCBM composite layer was determined by TEM analysis to be ~30 nm. To form top electrodes on top of the composite layer, a shadow mask with square patterns was aligned with front Al lines and a 50-nm-thick Au layer was deposited onto the substrate using an electron-beam evaporator. The device area of the organic memory was 0.5 mm × 1 mm. The hybrid-type 1D–1R devices consisting of an organic memory component (Al/PI:PCBM/Au) and an inorganic diode component (p-Si/Al) were then finally completed. All electrical measurements were made using a semiconductor characterization system (Keithley 4200-SCS) at room temperature in a N_2-filled glove box (see Figure S2 in the Supporting Information for details on device fabrication).

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