

# The application of conventional photolithography to microscale organic resistive memory devices

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## ABSTRACT

We demonstrate the application of conventional photolithography to fabricate organic memory devices in an array structure with a cell area of  $4 \times 4 \mu\text{m}^2$  without damaging the underlying organic memory layer. Applying photolithography to organic electronic devices is not trivial because the solvents used during lithography may dissolve and damage the previously coated organic layers. The application of photolithography to our organic devices was possible because of the introduction of polymethyl methacrylate (PMMA)/polyvinyl alcohol (PVA) onto the memory active layer, where PMMA functions as a buffer layer to prevent dissolution of the PVA layer during developing process, and PVA acts as a striped layer during metal lift-off process. Embedded Al bottom electrodes were particularly constructed to minimize the switching failure. The completed organic memory devices exhibited typical unipolar switching behavior and excellent memory performance in terms of their statistical memory parameters (ON and OFF currents and threshold voltages), ON/OFF ratio ( $>10^2$ ), endurance ( $>230$  cycles), and retention ( $>10^4$  s). This convenient photolithography patterning technique is applicable for the further scaling of many types of organic devices.

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## 1. Introduction

Organic resistive memory has been intensively studied because of its attractive technical characteristics, such as its flexibility, printability, and stackability [1–6]. It has been seriously considered as a candidate for data storage media for future flexible electronic applications [7–9]. The essential requirements for next-generation memory devices should include excellent memory properties, such as a nonvolatile memory effect, a high ON/OFF ratio, a fast switching speed, stable endurance, and long retention. Another important requirement is the ability to integrate as many cells as possible into a single chip. A crossbar type array structure, where the top electrode lines are vertically aligned with the bottom electrode lines, is a simple and efficient strategy to maximize the cell densities of organic memory devices (a single cell occupies  $4F^2$ , where  $F$  is the minimum feature size). Thus, this structure has been widely selected and demonstrated in previous studies [10–12].

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Conventional photolithography is a simple process for fabricating organic memory devices because it is well established and easily available. However, this process usually involves solvents for developing and removing the photoresist, which may dissolve the previously coated organic memory layers. Thus, organic memory devices have typically been fabricated by using patterned shadow masks, whose sizes are typically limited to 50  $\mu\text{m}$ . Alternatively, contact-based patterning techniques, such as microcontact printing ( $\mu\text{CP}$ ), nanoscale transfer printing (nTP), metal-transfer printing, and cold welding, have been demonstrated for structured organic memory devices with crossbar arrays [13–16]. However, technical limitations still exist, even for these techniques. For example,  $\mu\text{CP}$  requires an additional step to transfer self-assembled monolayer (SAM) ink [17]. Furthermore, SAM ink can spread laterally near the edges of the contact region, leading to inaccuracies during pattern scaling. Both nTP and cold welding require high pressures of over 300 MPa during metal transfer [14,16], which may damage the organic active layers. Recently, we reported direct metal transfer (DMT) as an alternative method to potentially avoid some of these technical drawbacks [12,18]. Although the DMT method is cost-effective, it is still not trivial to optimize the process conditions, which should differ depending on the organic materials used. Furthermore, almost all contact-based printing methods require

a perfectly flat morphology in the bottom electrodes to prevent the disconnection of the transferred top metal lines. As another alternative, a device with photolithographically patterned electrodes was previously demonstrated using a photocrosslinkable copolymer as an active layer for organic resistive memory devices [19]. However, the application of such a patterning method is also limited to crosslinking polymers with thermal and chemical robustness. Therefore, the application of conventional photolithography to make metal lines on top of organic materials is challenging for the aforementioned reasons, but it is still highly attractive. In addition, the device's scalability can be further enhanced with the progress of photolithography technology. Therefore, a novel patterning method based on conventional photolithography should be developed to solve these problems, enabling practical organic memory devices with high cell densities.

In this study, we demonstrated organic memory devices in an  $8 \times 8$  crossbar array structure with electrodes ( $4 \mu\text{m}$  line width) using conventional photolithography. Fabrication involves a bilayer film of polymethyl methacrylate (PMMA)/polyvinyl alcohol (PVA) on top of the organic memory active layer, where PMMA functions as a buffer layer to prevent the dissolution of the PVA layer during developing process, and PVA acts as a layer actually striped during metal lift-off. In particular, we fabricated embedded Al bottom electrodes to create a flat cell geometry that can minimize switching failures. The fabricated  $8 \times 8$  crossbar array organic memory devices exhibit typical unipolar switching behavior and excellent memory performance in terms of their statistical memory parameters (ON and OFF currents and threshold voltages), ON/OFF ratio, endurance, and retention.

## 2. Experimental

Fig. 1 shows the sequential fabrication of the  $8 \times 8$  crossbar array organic memory devices with embedded bottom electrodes using conventional photolithography. With the use of a positive photoresist, 8 trench lines were defined on a  $\text{SiO}_2$  ( $300 \text{ nm}$ )/Si substrate, and approximately  $50 \text{ nm}$  of  $\text{SiO}_2$  were then dry-etched using

a reactive ion etching system. Al was deposited to fill the trench. After lift-off, trench lines filled with Al were constructed. Fig. 1(a) shows a schematic of the bottom Al electrodes embedded in the  $\text{SiO}_2$  layer. We observed well-defined Al electrode lines through a scanning electron microscope (SEM) image (Fig. 2(a)). The Al lines had a  $4 \mu\text{m}$  line width and a  $22 \mu\text{m}$  distance (see Fig. 2(a), inset). We also examined the roughness of the embedded Al electrodes using an atomic force microscope (AFM). The surface morphology of a single Al line was observed, as shown in Fig. 2(b). A measured cross-sectional profile (its location indicated by a white dashed line in Fig. 2(b)) showed that the Al line electrodes were fabricated as a flat cell geometry, although they protruded slightly with respect to the neighboring  $\text{SiO}_2$  surface (see Fig. 2(b), inset plot). More accurate control during  $\text{SiO}_2$  etching and Al deposition would lead to flatter surface. To form an active organic layer in our resistive memory devices, biphenyltetracarboxylic acid dianhydride *p*-phenylene diamine (BPDA-PPD), which was used as a polyimide (PI) precursor, was dissolved in an *N*-methyl-2-pyrrolidone (NMP) solvent (BPDA-PPD:NMP = 1:3 by weight), and [6,6]-phenyl-C61 butyric acid methyl ester (PCBM) was also dissolved in the same solvent at a concentration of 0.5 wt %. A final composite PI:PCBM solution was prepared by mixing the PI solution (2 mL) with the PCBM solution (0.5 mL). The composite PI:PCBM solution was then spin-coated onto the substrate at 3000 rpm for 40 s (Fig. 1(b)). Before spin-coating with PI:PCBM, an  $\text{O}_2$  plasma treatment was applied to the samples, which improved the adhesion and enhanced the switching reproducibility [20]. The coated film was soft-baked on a hot plate at  $120 \text{ }^\circ\text{C}$  for 5 min to evaporate the solvent and then hard-baked in a nitrogen atmosphere at  $300 \text{ }^\circ\text{C}$  for 30 min. The thickness of the PI:PCBM composite layer was measured to be approximately 25 nm. In particular, thinner organic film on the protruding bottom structures can make step coverage poorer so that embedded bottom electrodes are necessary for our memory devices.

In particular, we found that the active PI:PCBM layer is vulnerable to the developer used during photoresist patterning, which renders photolithography difficult to use on an active polymer. To

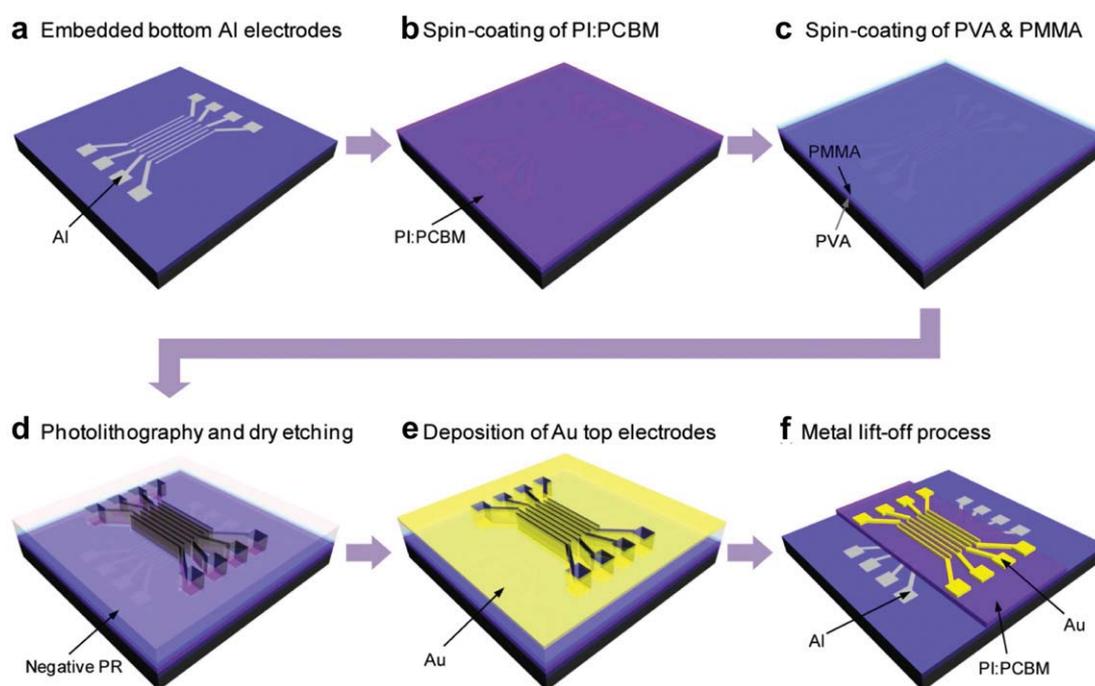
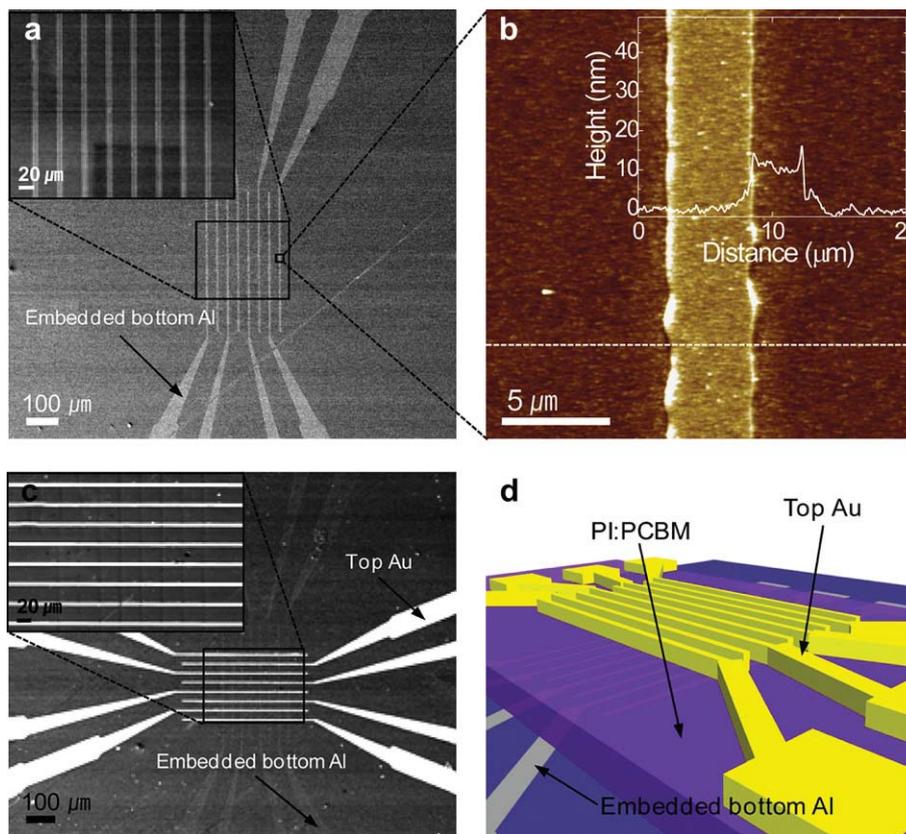


Fig. 1. The fabrication of organic memory devices with  $8 \times 8$  arrays and embedded bottom electrodes using conventional photolithography.



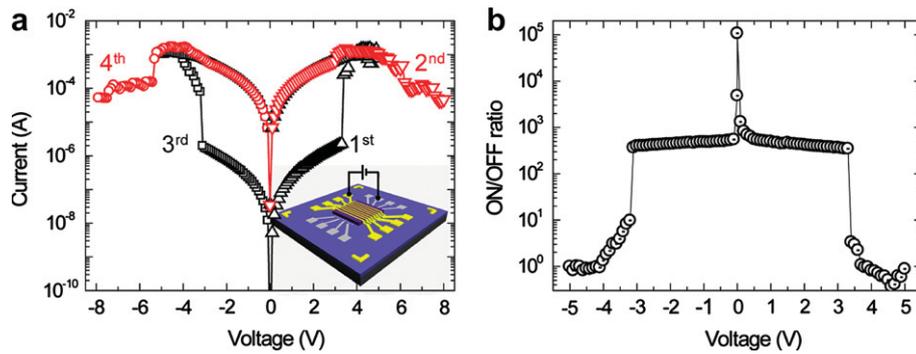
**Fig. 2.** (a) An SEM image of the embedded Al bottom electrodes. The inset shows an enlarged SEM image of 8 Al bottom lines. (b) An AFM image of an embedded Al bottom electrode line. The inset shows the cross-sectional topographic profile obtained from the white dashed line in the AFM image. (c) An SEM image of a completed Au/PI:PCBM/Al memory device with  $8 \times 8$  array cells. The inset shows an enlarged SEM image of the active region of the  $8 \times 8$  array. (d) A tilted schematic illustrating the smooth organic top surface resulting from the embedded Al bottom electrodes.

avoid such damage to the active PI:PCBM layer, we inserted a PMMA/PVA bilayer film before the photoresist coating. A water-soluble PVA polymer was used as a layer actually stripped during subsequent metal lift-off because the cured PI:PCBM layer is relatively resistant to water. However, the PVA was only weakly resistant to the MIF 300 developer of the negative photoresist. To prevent damage to the PVA layer during the developing process, an approximately 100-nm-thick PMMA interlayer was inserted between the PVA and the photoresist. The detailed process conditions were as follows: 4 wt % PVA dissolved in DI water was spin-coated onto the composite PI:PCBM layer at 4000 rpm for 50 s and baked at 80 °C; next, 4 wt % PMMA dissolved in chlorobenzene was spin-coated onto the PVA layer at 4000 rpm for 30 s and baked at 100 °C for 2 min (Fig. 1(c)). A negative photoresist was subsequently spin-coated onto the PMMA layer and was defined by 8 lines that were perpendicularly aligned with the bottom electrodes. This was followed by the dry etching of both the PMMA and PVA layers using O<sub>2</sub> plasma (Fig. 1(d)). As there was no etching selectivity between the two polymer layers, the etching process was performed based on etching rate of each layer (etch rates of 1.1, 0.4, and 1.4 nm/s for the photoresist, PMMA, and PVA, respectively) for the time necessary for removing the two layers. In particular, we selected a slow dry etching condition to minimize the unwanted etching of the active PI:PCBM layer. The thickness margin of the PI:PCBM film for reliable switching was verified to be between 15 and 25 nm. Next, an Au top metal layer was deposited onto the sample using an electron-beam evaporator (Fig. 1(e)). Metal lift-off was then used to strip the water-soluble PVA layer, which was removed using DI water (Fig. 1(f)). Particularly, metal etching

process could not be applied due to the limitation on the use of chlorine gas which is necessary for dry etching of Al metal. Furthermore, by-products generated during the dry etching process would detrimentally influence the switching characteristics. Finally, the Au/PI:PCBM/Al memory devices with  $8 \times 8$  array cells were completed, as shown in the SEM image in Fig. 2(c). The inset of Fig. 2(c) shows an image of 64 active cells with a junction area of  $4 \times 4 \mu\text{m}^2$ . The tilted schematic picture illustrates the smooth organic top surface (Fig. 2(d)), indicating that the spin-coating of the PI:PCBM composite was not dramatically hindered by the bottom electrode architecture. Generally, the surface of the spin-coated PI:PCBM organic layer follows the morphology of the bottom electrodes patterned on the substrate, which determines the geometry of the cross-junction memory cell. The Yang group has suggested that the switching sites introduced by any nonflat geometry must be better controlled to overcome this inconsistency and render the polymer memory devices more reproducible and reliable [21,22]. Therefore, an embedded bottom electrode architecture would be more favorable in terms of switching reproducibility and reliability of such memory devices.

### 3. Results and discussion

To electrically characterize the fabricated memory devices, we measured the current–voltage (*I*–*V*) characteristics of the Au/PI:PCBM/Al devices using a semiconductor characterization system (Keithley 4200-SCS) in an N<sub>2</sub>-filled glove box at room temperature. Positive voltages were applied to the top electrode (Au), and the bottom electrode (Al) was grounded. Fig. 3(a) shows the *I*–*V*

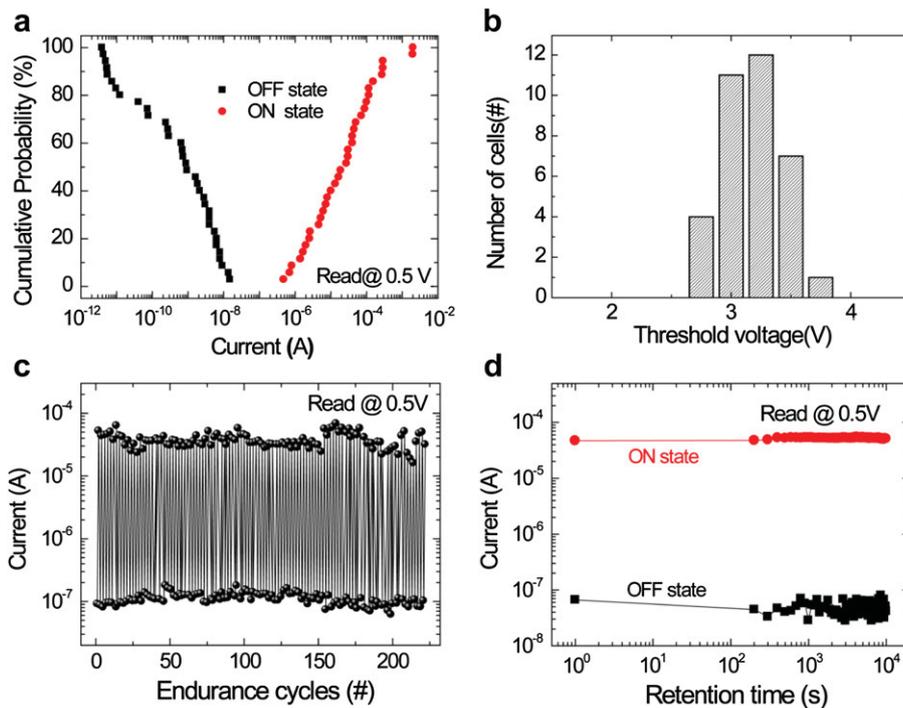


**Fig. 3.** (a) The I–V characteristics of an Au/PI:PCBM/Al memory device. The inset shows the positive and negative voltage polarity applied to the top and bottom electrodes of the device, respectively. (b) The ON/OFF ratio as a function of the voltage.

characteristics of a memory device on a semilogarithmic scale. When voltages (from 0 to 5 V) were applied to the device in double-sweep mode (1st), the current initially remained low, indicating a high-resistance state (HRS, OFF state), and then suddenly switched to a low-resistance state (LRS, ON state) near  $\sim 3$  V. During the recovery from 5 V back to zero, the current remained in the ON state, representing the nonvolatile memory effect. When voltages (from 0 to 8 V) were applied to the device in single-sweep mode (2nd), the ON state remained in the low-voltage region, and then the current gradually decreased over 4 V, which is associated with erasing. Based on these results, the operating voltages for writing, erasing, and reading could be determined to be  $\sim 5$ , 8, and 0.5 V, respectively. Our memory devices exhibited unipolar switching behavior, in which writing and erasing operated under the same voltage polarity [23,24]. Current bistability was also observed in the negative voltage polarity (3rd and 4th), exhibiting electrically symmetric I–V behavior. In particular, unipolar memory switching is an important trait for practical memory applications since electrically rewritable switching property in one-diode and

one-resistor (1D–1R) array architecture, which prevents cross-talk interferences occurring between neighboring cells, is only available by the use of unipolar switching memory devices [23]. Another merit is that the external circuit necessary for practical memory applications can be simplified due to the use of a single voltage polarity. In terms of these points, further work would be put on the development of the 1D–1R array structure. In previous studies, the resistive switching of the PI:PCBM composite was due to the introduction of PCBM molecules, which might act as charge-trapping sites [23,25]. This resistive switching phenomenon may be associated with the charge-trapping/detrapping mechanism described by Simmons and Verderber [26] and Bozano et al. [27,28]. Fig. 3(b) shows the ON/OFF ratio as a function of the applied voltage. This memory device showed a high ON/OFF ratio (over  $10^2$  within 3 V; Fig. 3(b)). This was sufficiently large to distinguish the ON and OFF states.

It is essential to statistically evaluate the memory parameters of the operating cells in array-type memory devices. Fig. 4(a) shows the cumulative probability data of each of the current states (ON



**Fig. 4.** (a) The cumulative probabilities of the ON and OFF states obtained from 35 randomly selected operating memory cells. (b) A histogram of the threshold voltages. (c) The endurance cycles of an Au/PI:PCBM/Al device in I–V sweep mode. (d) The retention time of an Au/PI:PCBM/Al device.

and OFF) of 35 selected cells. Although each state was distributed across a wide range, we could observe a gap of more than one order of magnitude between the ON and OFF states. Fig. 4(b) shows the threshold voltage distribution extracted from the I–V plots of the 35 measured cells. The threshold voltages for writing to the memory cells were distributed in a range between 2.5 and 4 V. Because the value of the threshold voltage is usually related to the thickness of the active layer [29], it would be critical to accurately control the thickness of the PI:PCBM layer that remains after dry etching.

Endurance cycling data were also obtained from a repetitive I–V sweep test of a single cell (Fig. 4(c)). During 230 sweep cycles, each current state of the memory device remained stable, with no serious electrical fluctuations. There were no switching failures during the endurance cycling test, which exhibited excellent rewritable switching properties. Such stable endurance was achieved by the embedded bottom electrode architecture, which eliminated the unwanted leakage current path through the edge of the cross-junction region [30]. To evaluate their ability to retain information, the retention time of each current state was measured, as shown in Fig. 4(d). The memory device exhibited a long retention time of  $10^4$  s. The actual lifetimes of the devices can be much longer than the retention time evaluated, indicating good performance in terms of their information storage capability.

#### 4. Conclusions

In this work, we demonstrated organic memory devices with a cell size of  $4 \times 4 \mu\text{m}^2$  that were fabricated using a simple patterning method based on conventional photolithography. The application of photolithography was possible by introducing a PMMA/PVA bilayer film to prevent chemical damage to the active PI:PCBM memory layer that would have otherwise been caused by the strong solvents that are necessary during fabrication. Embedded Al bottom electrodes were particularly made to minimize switching failure by eliminating the unexpected leakage current path through the edge of the memory cell junctions. Our organic memory devices showed typical unipolar switching behavior and excellent memory performance in terms of their statistical memory parameters, endurance, and retention.

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