

# Morphology- and Orientation-Controlled Gallium Arsenide Nanowires on Silicon Substrates

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## ABSTRACT

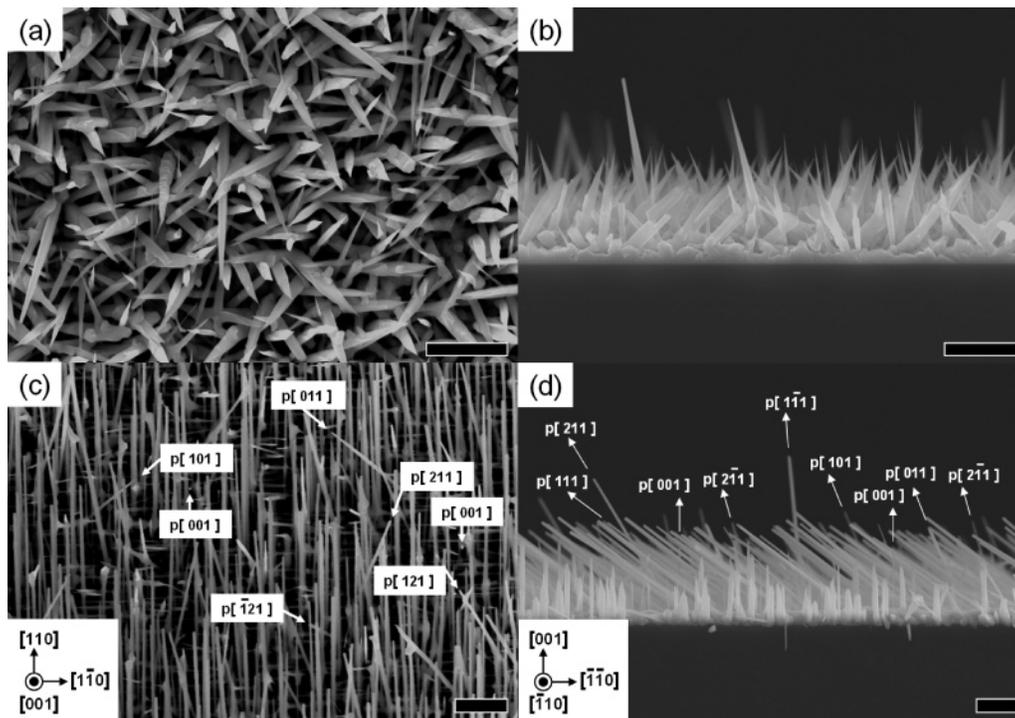
GaAs nanowires were epitaxially grown on Si(001) and Si(111) substrates by using Au-catalyzed vapor–liquid–solid (VLS) growth in a solid source molecular beam epitaxy system. Scanning electron microscopy analysis revealed that almost all the GaAs nanowires were grown along  $\langle 111 \rangle$  directions on both Si substrates for growth conditions investigated. The GaAs nanowires had a very uniform diameter along the growth direction. X-ray diffraction data and transmission electron microscopy analysis revealed that the GaAs $\langle 111 \rangle$  nanowires had a mixed crystal structure of the hexagonal wurtzite and the cubic zinc-blende. Current–voltage characteristics of junctions formed by the epitaxially grown GaAs nanowires and the Si substrate were investigated by using a current-sensing atomic force microscopy.

Nanowires (nanorods or nanowhiskers) have been attracting a great deal of attention as a one-dimensional nanostructure due to their easily tailored chemistry. Nanowires can be grown from various materials including semiconductors by utilizing various material growth systems including pulsed-laser deposition (PLD), metal–organic chemical vapor deposition (MOCVD), chemical beam epitaxy (CBE), and molecular beam epitaxy (MBE) systems. Among them, MOCVD and CBE system are widely used for nanowire growth. However, in general nanowires grown by MOCVD or CBE system using vaporized chemical sources are tapered due to the higher lateral growth rate under high-pressure conditions.<sup>1–3</sup> The taper of nanowires is potentially a significant problem for device applications since the change of their diameter can significantly change the electronic and optical properties of the nanowires. To solve this problem, Greytak et al.<sup>4</sup> employed a reduced temperature elongation growth and Wu et al.<sup>5</sup> employed an MBE. Greytak et al. demonstrated CVD-grown Ge nanowires having a uniform diameter by introducing a low-temperature elongation step after a high-temperature nucleation step. Wu et al. could

dramatically suppress the lateral growth of nanowires due to the limited availability of source materials on the side walls of the nanowires thanks to the ultrahigh vacuum condition and the strong directionality of the source beams in an MBE. With these growth techniques, semiconductor nanowires for future electronic and photonic nanodevice applications including resonant tunneling diodes,<sup>6</sup> field effect transistors,<sup>7,8</sup> single electron transistors,<sup>9</sup> and light emitting diodes<sup>10,11</sup> have been actively studied.

Integration of compound semiconductor devices having superior optoelectronic properties with well-established Si integrated circuits has been an everlasting issue. Epitaxial growth of III–V semiconductor layers on Si substrates for monolithic integration has been hindered by fundamental problems including the mismatch in lattice constant, the difference in thermal expansion coefficient, and the disparate crystal structure forming antiphase boundaries (APBs). Growth of III–V compound semiconductors in the form of nanowires by using a nanoparticle-catalyzed vapor–liquid–solid (VLS) growth<sup>12</sup> can nearly avoid these problems. In the VLS growth of nanowires, the stress induced by the lattice constant mismatch is relieved at the surface of the side wall of the nanowire<sup>13</sup> and their small growth area

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**Figure 1.** Morphologies of GaAs nanowire samples grown on Si(001) substrates for 40 min imaged by an FESEM. (a) Plan view and (b) cross-sectional view of the sample grown at 480 °C with V–III ratio of 5. (c) Plan view and (d) cross-sectional view of the sample grown at 580 °C with V–III ratio of 9. The insets represent the directional indices, where [001] represents the direction of the Si substrate normal. Some wires are marked with the arrows and the growth directions represented by p[growth direction]. All scale bars are 2  $\mu\text{m}$  long. Abnormally thick nanowires shown in front of Figure 1d are the GaAs wires grown at the edge of the cleaved Si(111) substrate and thus should be excluded from analysis. The SEM images of the samples in panels c and d were slightly tilted about the [1 $\bar{1}$ 0] axis and the [001] axis, respectively, and thus neither the [001] nor the [1 $\bar{1}$ 0] is completely normal to the projection planes.

remarkably reduces the probability of the formation of APBs. While there were many reports on homoepitaxial growth of nanowires on bulk substrates for various material systems including Si,<sup>14,15</sup> Ge,<sup>16,17</sup> GaAs,<sup>1</sup> InP,<sup>18</sup> and InAs,<sup>2</sup> epitaxial growth of III–V semiconductor nanowires on Si substrates was rarely demonstrated except for the growth of GaP, GaAs, and InP nanowires on Si substrates by Mårtensson et al. using an MOCVD.<sup>19</sup>

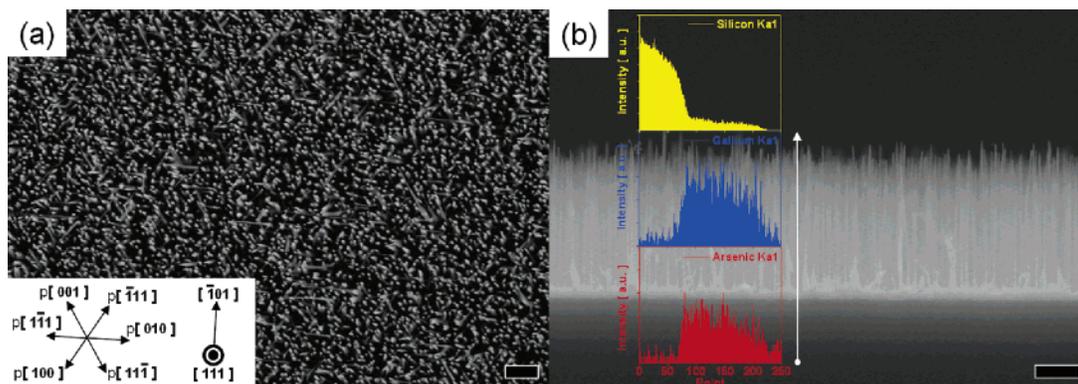
In this paper, growth of substrate-oriented GaAs nanowires having a uniform diameter along the growth direction on Si(001) and Si(111) substrates by using Au-catalyzed VLS growth in a molecular beam epitaxy is presented.

The GaAs nanowires were grown by using a VG V80H-10K solid source MBE (SSMBE) system equipped with a valved-cracker arsenic cell on cleaved Si(001) and Si(111) substrates having the area of approximately 400 mm<sup>2</sup>. The Si substrates were degreased and then immersed in a diluted hydrogen fluoridic acid solution (1%) for removal of native oxides. After the oxide removal, the Si substrates were instantly loaded in an electron beam evaporator for deposition of an Au film (4 Å). The Au-deposited Si substrates were then transferred into the MBE growth chamber and annealed at 540 °C for 10 min to form Au nanoislands. After the substrate temperature ( $T_s$ ) was changed to the target growth temperature, arsenic and gallium sources were supplied for the wire growth. The growth was terminated by closing the shutter for the gallium effusion cell while maintaining the valve for the arsenic cracker cell open until the substrate

temperature fell below 300 °C to avoid arsenic decomposition from the GaAs surface.

Various MBE growth conditions (substrate temperatures between 480 and 640 °C and V–III ratios between 3 and 20) were examined for the GaAs nanowire growth with a fixed gallium beam flux required for the homoepitaxial GaAs growth rate of 0.9  $\mu\text{m}/\text{h}$  on a GaAs(001) substrate. The MBE-grown GaAs nanowires on Si(111) and Si(001) substrates were characterized by using a Hitachi S-4700 field-emission scanning electron microscopy (FE-SEM).

Panels a and b of Figure 1 show the plan view and the cross-sectional view SEM images of the sample grown on a Si(001) substrate at 480 °C with the V–III ratio ( $V/III$ ) of 5, respectively. As shown in the figures, the wires are significantly tapered and random in growth direction. Similar growth results were observed in the samples grown at the growth temperatures ( $T_s$ ) below 500 °C with the  $V/III$  smaller than 5–9 (dependent on  $T_s$ ). The tapering of nanowires at low growth temperature is attributed to the reduced diffusion of the growth species on the sidewall of the GaAs nanowire.<sup>20</sup> In contrast, as shown in parts c and d of Figure 1, most of the nanowires grown on a Si(001) substrate at 580 °C with the  $V/III$  of 9 have a uniform diameter along the wire axis and are either parallel or perpendicular to each other, indicating that they are the  $\langle 111 \rangle$  family in growth direction and thus are epitaxially grown nanowires. It was observed that Au-catalyzed GaAs nanowire epitaxy by using the SSMBE system on Si(001) substrates having a uniform



**Figure 2.** Morphologies of GaAs nanowire samples grown on Si(111) substrates imaged by an FESEM. (a) Plan view and (b) cross-sectional view of the sample grown at 580 °C with the V–III ratio of 11 for 20 min. The inset in Figure 2a schematically represents the projections of GaAs nanowires grown along the three different  $\langle 111 \rangle$  directions and three different  $\langle 001 \rangle$  directions on the (111) Si surface plane, which are represented by p[growth direction]. The insets in Figure 2b are the results of the SEM-based XEDS line scan along the wire axis showing the boundary of the Si substrate and the GaAs nanowires. All scale bars are 1  $\mu\text{m}$  long.

diameter along the wire can be achieved for the substrate temperature range from 530 to 580 °C and the V–III ratios larger than 5–9 (depending up on the substrate temperature). Projections of the GaAs nanowires grown along various directions are indicated in parts c and d of Figure 1, where SEM images of the sample were slightly tilted about the  $[1\bar{1}0]$  axis and the  $[001]$  axis, respectively. Note that GaAs nanowires having different growth directions including  $\langle 011 \rangle$  and  $\langle 112 \rangle$  families as well as  $[001]$  can be occasionally observed. The GaAs $\langle 011 \rangle$  nanowires on a GaAs $\langle 001 \rangle$  substrate have been already reported by Wu et al.<sup>5</sup> However, to the best of our knowledge, the GaAs $\langle 112 \rangle$  and GaAs $\langle 001 \rangle$  nanowires have not been reported yet due to their scarceness. However, they can be observed in the plan-view SEM image given by Wu et al. in ref 5, even though they did not mention them.

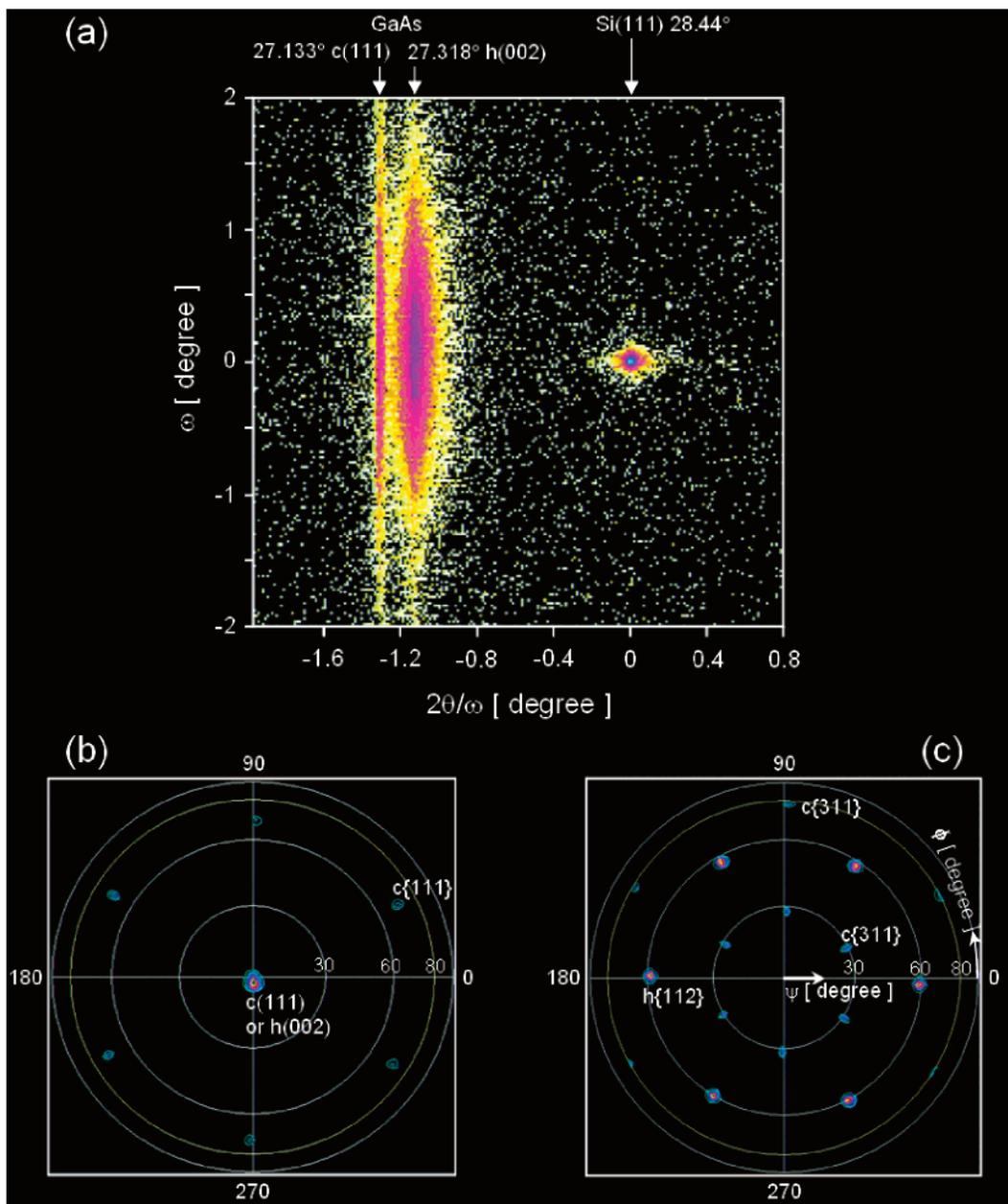
Growth of GaAs nanowire on Si(111) substrates was carried out for the substrate temperatures between 530 and 580 °C and V–III ratios between 9 and 11. Parts a and b of Figure 2 show the plan view and the cross-sectional view SEM images of the GaAs nanowires grown on Si(111) substrates at 580 °C with the V–III ratio of 11, respectively. Since most GaAs nanowires were grown vertically from the Si(111) substrate, they are projected as spots as shown in Figure 2a. Other nanowires projected as lines were grown in one of the  $\langle 111 \rangle$  family as represented in the inset. Unlike GaAs nanowires grown on Si(001) substrates, GaAs nanowires grown along other than  $\langle 111 \rangle$  direction cannot be observed. As can be seen in the cross-sectional view, GaAs nanowires were uniform along the growth direction. The insets of the Figure 2b show the results of the SEM-based X-ray energy-dispersive spectrometer (XEDS) line scan along the growth direction. The arrow from the Si(111) substrate to the tips of the GaAs nanowires represents the trace of the XEDS line scan. The boundary of the Si substrate and the GaAs nanowires is clearly shown.

In order to further confirm that GaAs nanowires on the Si(111) substrate are epitaxially grown, X-ray diffraction (XRD) measurements were carried out using a four-axis diffractometer (PANalytical X'Pert MRD). A typical out-

of-plane symmetric  $2\theta/\omega$ -scan using hybrid optics that consist of a double crystal Ge(220) monochromator and a graded multilayer mirror was performed. There are no peaks observed within the whole scan range (from 20° to 80°, not shown here) except for the Si(111) peak at 28.44° and one broad peak at 27.308° possibly indexed as the GaAs (111) diffraction peak. Although this result already indicates that the GaAs nanowires were epitaxially grown, we carried out a reciprocal space mapping (RSM) by the high-resolution X-ray diffraction with a four crystal Ge(220) monochromator, a graded multilayer mirror, and an analyzer crystal in order to get more detailed information.

Figure 3a shows the RSM for the GaAs nanowires grown on a Si(111) substrate. As shown in Figure 3a, the peak at 27.308° obtained through the out-of-plane  $2\theta/\omega$ -scan was split into two peaks at 27.133° and 27.318° in the higher resolution RSM. We inferred that the peaks at 27.133° and 27.318° corresponded to the cubic (111) and the hexagonal (002) planes, respectively, because the Bragg angles of the cubic zinc-blende GaAs(111) and the hexagonal wurtzite GaAs(002) planes are close to each other around 27° ( $2\theta$ ). The presence of the two peaks indicate that the individual GaAs nanowire grown on Si(111) substrates has the mixed crystal structure consisting of cubic zinc-blende and hexagonal wurtzite structures or there are two kinds of GaAs nanowires having one of the two different structures. The broadness of the two peaks in the rocking angle ( $\omega$ -axis) is ascribed to the slight tilts of the individual GaAs nanowires as shown in Figure 2b.

In order to verify the two crystal structures in the GaAs nanowires on the Si(111) substrate, we performed XRD pole figure measurements. Figure 3b is the out-of-plane pole figure measured near the cubic GaAs(111) or hexagonal GaAs(002) Bragg angle ( $2\theta = 27.15^\circ$  in this measurement). The six peaks at  $\sim 70.5^\circ$  (the inclination angle  $\psi$ , i.e., the tilt about the out-of-plane) separated by the azimuthal rotation angle ( $\phi$ ) of 60° can be observed only from the cubic zinc-blende GaAs $\{111\}$  reflection planes. The peak at the center can be obtained from the cubic zinc-blende GaAs(111) and the hexagonal wurtzite GaAs(002). In order to confirm the

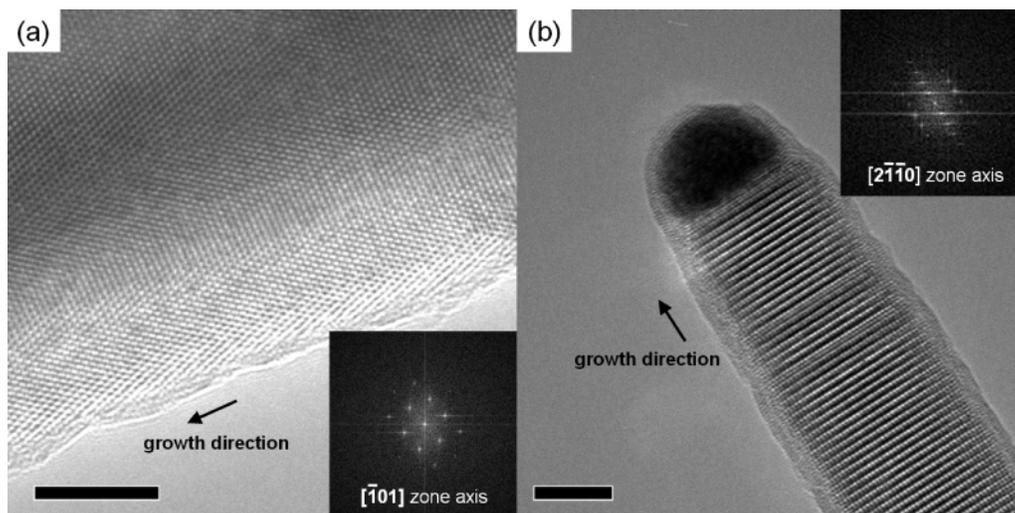


**Figure 3.** XRD data obtained from the GaAs nanowires grown on the Si(111) substrate: (a) the out-of-plane reciprocal space map; (b) the pole figure obtained near the cubic GaAs(111) or hexagonal GaAs(002) Bragg angle ( $2\theta = 27.15^\circ$  in this measurement); (c) the pole figure obtained near the cubic (311) or hexagonal (112) Bragg angle ( $2\theta = 53.76^\circ$ ). The peak of the Si(111) substrate is set at  $0^\circ$  in both  $\omega$ - and  $2\theta/\omega$ -axes (Figure 3a).

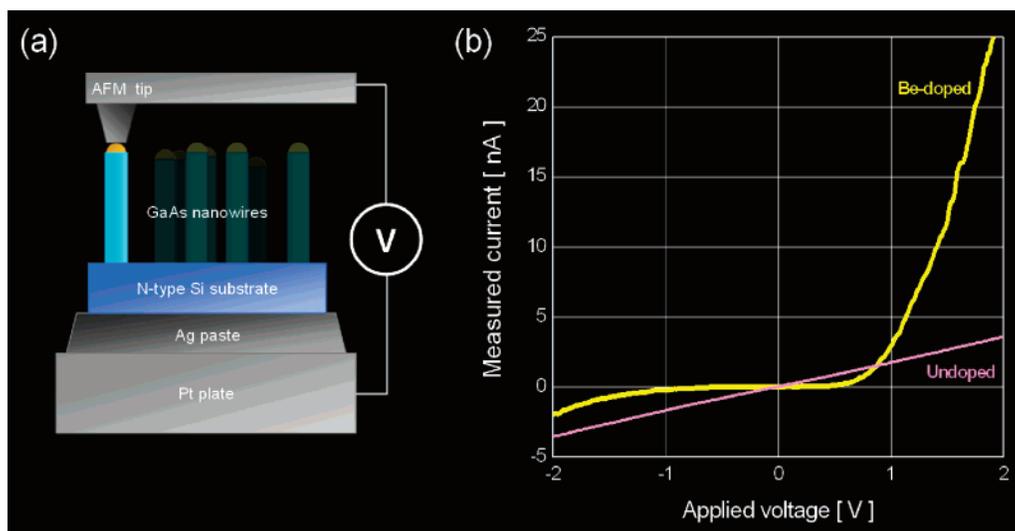
presence of the hexagonal wurtzite structure in the GaAs nanowires, another XRD pole figure measurement was performed near the hexagonal GaAs(112) and cubic GaAs-(311) Bragg angle ( $2\theta = 53.76^\circ$  in this measurement). Figure 3c shows this pole figure confirming the existence of the hexagonal wurtzite structure. The peaks at the inclination angles ( $\psi$ ) of approximately  $29.5^\circ$  and  $80.0^\circ$  separated by the azimuthal rotation angle ( $\phi$ ) of  $60^\circ$  are obtained from the cubic GaAs{311} reflection planes, while the peaks at the inclination angles of approximately  $58.7^\circ$  separated by the azimuthal rotation angle of  $60^\circ$  are from the hexagonal GaAs(112). The relative position of the spots indicates that the cubic GaAs{311} is rotated  $30^\circ$  with respect to the hexagonal GaAs(112). These results clearly indicate that the

GaAs nanowires grown on Si(111) substrates have both the cubic zinc-blende and the hexagonal wurtzite structures. From all these XRD data of the MBE-grown GaAs nanowires on Si(111) substrates, we can conclude that the GaAs hexagonal phase is present with (002) parallel to cubic GaAs-(111) and perpendicular to the growth direction of the wires.

High-resolution transmission electron microscopy (HRTEM) images were obtained from the GaAs nanowires dispersed on a carbon-film-coated copper grid from the same sample through a sonication. An extensive HRTEM image analysis revealed that most of the GaAs(111) nanowires grown on Si(111) substrates have a pure single crystalline structure without any line defects such as dislocations or grain boundaries, although some HRTEM images showed partially



**Figure 4.** High-resolution TEM images of GaAs $\langle 111 \rangle$  nanowires dispersed from the Si(111) substrate by a sonication, which were grown at 580 °C with V–III ratio of 11 for 5 min. (a) A GaAs $\langle 111 \rangle$  nanowire having the cubic zinc-blende structure (ZB) and no line defects such as stacking faults, grain boundaries, or dislocations. (b) A GaAs $\langle 111 \rangle$  nanowire mainly having the hexagonal wurtzite structure (WZ) with stacking faults resulting in the crystal change from WZ to ZB or from ZB to WZ. The insets are the results of the two-dimensional fast Fourier transforms indicating that the zone axes are  $[101]$  and  $[11\bar{2}0]$ , respectively. All scale bars are 5 nm long.



**Figure 5.** (a) Schematic of the current-sensing AFM measurement and (b) current–voltage characteristics of undoped and Be-doped GaAs nanowires grown on n-type ( $n = 2 \times 10^{18}/\text{cm}^3$ ) Si(001) substrates obtained from the current-sensing AFM measurements.

the mixed crystal structures consisting of zinc-blende and wurtzite structures. Panels a and b of Figure 4 show the GaAs $\langle 111 \rangle$  nanowires that have the pure zinc-blende structure and the mixed crystal structure consisting of zinc-blende and wurtzite structures, respectively. The mixed crystal structure in GaAs (and InAs) nanowires epitaxially grown on bulk GaAs and InAs substrates by using MOCVD, respectively, was already reported by Hiruma et al.<sup>3</sup> Similar to our GaAs- $\langle 111 \rangle$  nanowires grown on Si(111) substrates, they were formed through alternation of the zinc-blende and the wurtzite structures with stacking faults in between, which is usually observed in the VLS growth.<sup>3</sup> The insets of parts a and b of Figure 4 show the results of the two-dimensional fast Fourier transforms indicating that the zone axes are  $[101]$  and  $[11\bar{2}0]$ , respectively. They reveal that the growth

directions of the two GaAs nanowires are  $[111]$  and  $[0001]$  (parallel), respectively.

Electrical characteristics of the epitaxially grown GaAs nanowires combined with the Si substrates were investigated by using current-sensing atomic force microscopy (AFM) measurements.<sup>21–23</sup> Figure 5a is the schematic diagram for the AFM-based current measurement setup. A Pt/Ir coated n-type Si AFM tip was scanned in the contact mode while a variable dc voltage was applied simultaneously between the AFM tip and the backside of the Si substrate bonded to a Pt plate via an Ag paste. The current was measured when electrical contact between the AFM tip and a tip of a single nanowire was formed. The contact area, which was calculated based on Johnson–Kendall–Roberts<sup>24</sup> model with the AFM tip radius (40 nm) and the loading force (10 nN), was 100

nm<sup>2</sup>. Figure 5b shows measured current–voltage characteristic curves for undoped and Be-doped GaAs nanowires grown on n-type ( $n = 2 \times 10^{18}/\text{cm}^3$ ) Si(001) substrates. For the undoped GaAs nanowires, linear and symmetric curves (typical ohmic characteristic curves) were obtained and their resistances values ranged from 561 to 850 M $\Omega$ . The ohmic characteristics are attributed to the unintentional doping during the GaAs nanowire growth on Si substrates. Note that, although the doping level is very low ( $10^{14}$ – $10^{15}$  cm<sup>-3</sup>), undoped GaAs layers grown by bulk epitaxial layer growths is also unintentionally n-type doped. In the case of the Be-doped GaAs nanowires, current–voltage characteristic curves showed a diode-like nonlinear behavior, indicating that a p–n junction was successfully formed between the Be-doped GaAs nanowire and the n-type Si substrate.

In summary, epitaxial growths of GaAs nanowire on Si substrates by using an SSMBE were investigated. SEM and XRD analysis showed that the GaAs nanowires having an almost identical orientation and a uniform diameter along the growth direction can be grown. XRD pole figure measurements and HRTEM images showed that the GaAs nanowires had the cubic zinc-blende structure or hexagonal wurtzite structure, or mixture of the two structures. HRTEM images also showed the high crystalline quality of the GaAs nanowires grown on Si substrates. AFM-based current–voltage measurements showed that undoped and Be-doped GaAs nanowire grown on an n-type Si substrate had p–n diode and ohmic characteristics, respectively. These results indicate the potential of the MBE-based III–V semiconductor nanowire epitaxy on Si substrates for use in direct integration of high-performance III–V compound semiconductor nanoscale devices with the main stream Si technology.

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