Effects of channel-length scaling on In_2O_3 nanowire field effect transistors studied by conducting atomic force microscopy

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Scaling effects of In_2O_3 nanowire field effect transistors (FETs) were examined as a function of channel length. The channel length was varied from 1 μm to 20 nm by placing a conducting atomic force microscope tip on the In_2O_3 nanowire as a movable contact. The In_2O_3 nanowire FET exhibited a variety of channel-length dependent transfer characteristics in terms of the source-drain current, transconductance, threshold voltage, and mobility. Furthermore, the authors were able to extract the contact resistance and distinguish between apparent mobility and intrinsic mobility. The latter was corrected, taking into account the non-negligible contact resistance for short channel devices. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2728754]

Metal oxide nanowires such as ZnO, SnO_2, CdO, and In_2O_3 have been extensively studied in terms of their potential applications in electronic, photonic, and biological sensing devices.[1–6] Of these, In_2O_3 nanowires have been widely used as nanoelectronic building blocks for nanoscale transistors,[7] memory devices,[8] and sensors.[6] However, the majority of current research regarding In_2O_3 and other metal oxide nanowires typically focuses on the synthesis of diameter-controlled nanowires and device applications such as nanowire field effect transistors (FETs) with micron-sized channel lengths. To this end, the scaling effects of nanowire FETs have not yet been extensively examined, as compared with conventional metal oxide semiconductor field effect transistors (MOSFETs).[9] As such, it is important to explore the dependence of the electrical properties of nanowire FET devices on channel length prior to developing applications in the area of highly integrated nanowire electronics.

In this letter, we report on a study of the scaling effects of In_2O_3 nanowire FETs as a function of channel length. In this study, the channel length was altered by placing a conducting atomic force microscopy (CAFM) tip at various positions along an In_2O_3 nanowire. Then, by subsequent measurements and an analysis of the transfer characteristics for different channel lengths, we investigated the scaling effects of the source-drain current, transconductance, threshold voltage, and mobility with respect to channel length. We also investigated the issue of how mobility is influenced by non-negligible contact resistance for short channel-length nanowire FETs.

The In_2O_3 nanowires used in this study were prepared by carbothermal reduction followed by a catalyst-mediated heteroepitaxial growth technique. A detailed description of the synthesis of In_2O_3 nanowires has been reported elsewhere.[10] Figure 1(a) shows a typical field-emission scanning electron microscopy (FE-SEM) image of In_2O_3 nanowires grown on the Si/SiO_2 substrate. As can be seen, the nanowires have a diameter in the range of 10–100 nm and a length extending to 5 μm or more, as determined by SEM and transmission electron microscopy (TEM) analyses. Note that the high-resolution TEM (HRTEM) image shown in Fig. 1(b) indicates that the In_2O_3 nanowire is a single crystalline material with an interplanar spacing of 0.5 nm in the [100] direction. The electron diffraction pattern was recorded along the ⟨001⟩ zone axis, as shown in the inset of Fig. 1(b).

In order to characterize the electrical properties of In_2O_3 nanowires, we fabricated In_2O_3 FETs by optical lithography. Here, metal electrodes, consisting of Ti (30 nm)/Au (50 nm), were deposited on top of an In_2O_3 nanowire by an electron beam evaporator followed by lift-off. A highly doped silicon substrate with an oxide thickness of 100 nm was used as a common back-gate electrode to modulate the carrier density in the nanowire. Then, to investigate the channel-length dependent transfer characteristics of In_2O_3 nanowire FETs, we used the Pt-coated tip of a CAFM as a movable drain electrode on the nanowire, as schematically illustrated in Fig. 1(c).[11] In this study, the channel length of the In_2O_3 nanowire FET was varied from 1 μm to 20 nm. When the Pt-coated CAFM tip made physical contact at a controllable position on the nanowire, a drain bias V_{DS} was applied to the CAFM tip relative to the source electrode. The resulting source-drain current I_{DS} was measured with a cur-

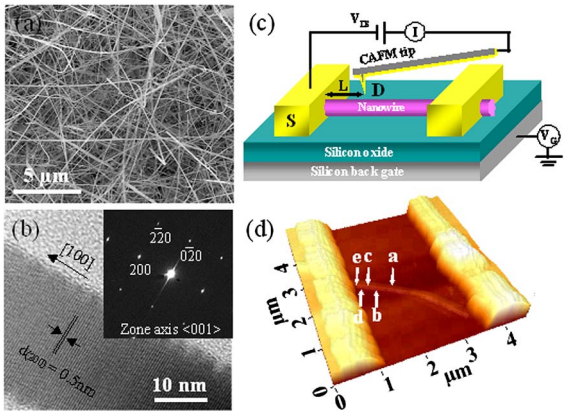

FIG. 1. (Color online) (a) FE-SEM image of In_2O_3 nanowires grown on a Si/SiO_2 substrate. (b) HRTEM image of an In_2O_3 nanowire. The inset shows an electron diffraction pattern. (c) Schematic of the CAFM setup for characterizing an In_2O_3 nanowire FET. (d) AFM image of the In_2O_3 nanowire FET device characterized in this study. The channel length of the device was varied by moving the CAFM tip to five different positions (a=1 μm, b=500 nm, c=200 nm, d=50 nm, and e=20 nm).

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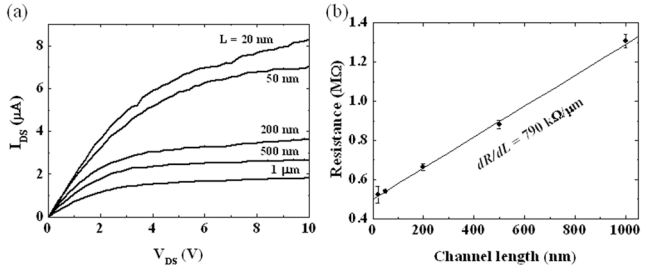

FIG. 2. (a) V_{DS}-I_{DS} characteristics for various channel lengths at zero gate bias. (b) Resistance vs channel length for an In_2O_3 nanowire FET.

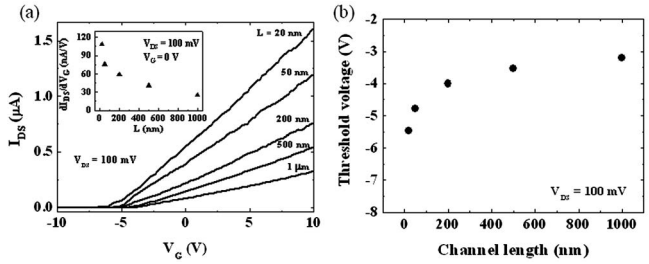

FIG. 3. (a) I_{DS}-V_G characteristics for various channel lengths at fixed V_{DS} =100 mV. The inset shows transconductance dI_{DS}/dV_G versus channel length. (b) Threshold voltage vs channel length.

rent amplifier attached to the CAFM tip in an ambient atmosphere. Figure 1(d) shows the AFM image of the In_2O_3 nanowire FET device used in this study (diameter of ~25 nm). The CAFM tip was positioned on the nanowire at specific locations (a=1 μm, b=500 nm, c=200 nm, d=50 nm, and e=20 nm). Note that the AFM image [Fig. 1(d)] was obtained after the completion of the CAFM experiments in order to avoid potential damage to the nanowire by the CAFM tip.

Figure 2(a) presents the source-drain current versus drain voltage (I_{DS}-V_{DS}) characteristics of the In_2O_3 nanowire FET, obtained at a zero gate bias for channel lengths L of 1000, 500, 200, 50, and 20 nm corresponding to positions a to e, as shown in Fig. 1(d). On the drain electrode side, the Pt CAFM tip on a n-type In_2O_3 nanowire generally forms a Schottky barrier. However, Ohmic behavior can be achieved from the small contact area of the sharp CAFM tip since a high electric field is induced on the top of the In_2O_3 surface by the sharp curvature of the tip, which leads to a narrowing of the Schottky barrier width and, as a result, Ohmic contact behavior.[12] It has been reported that Ti produces Ohmic contact on In_2O_3 nanowires at room temperature on the source electrode side due to a sufficiently low Schottky barrier height.[7] Corresponding I_{DS}-V_{DS} curves recorded for short channel lengths of 20 and 50 nm exhibited positive slopes in the saturation regime under the positive drain bias applied to the CAFM tip, as shown in Fig. 2(a). The continued current increase after the saturation regime is similar to short channel effects due to channel-length modulation (CLM) found in conventional MOSFETs and Schottky barrier MOSFETs with short channel length.[13] The CLM effect in short channel MOSFETs explains the current increase after the saturation regime as the increase in the electric field in the reduced effective channel caused by an increase in the depletion region on the drain side (for example, n^+-p junction for n-channel conventional MOSFETs and metal/p-type semiconductor for n-channel Schottky barrier MOSFETs). In the case of the Pt CAFM tip on the In_2O_3 nanowire at the drain electrode, since the width of the Schottky barrier on the drain side is narrowed by the application of a positive drain bias, the contact resistance can be reduced, resulting in a less voltage drop across the Schottky barrier and a higher voltage drop across the channel in excess of the saturation drain voltage. As this field increases, the current density through the region must also increase to satisfy Ohm's law. Therefore, the short channel effects in our nanowire FET can also be explained with CLM effect like the conventional MOSFETs, which is based on the variation of the channel length and the increase of the electric field with an increase in drain bias.

For low drain biases, the I_{DS}-V_{DS} characteristics appear linear, and the low bias resistance R_{tot} (obtained by linear fitting from 0 to 0.6 V) is plotted for different channel lengths in Fig. 2(b). Note that the resistance R_{tot} is the sum of two resistances: nanowire channel resistance R_{NW} and contact resistance R_C between the electrodes and the nanowire. The total device resistance $R_{tot}=V_{DS}/I_{DS}$ is plotted as a function of channel length L for zero gate voltage, as shown in Fig. 2(b). The parasitic contact resistance R_C was determined to be 500±20 kΩ by extrapolating the channel length to zero. The channel resistance R_{NW} varies linearly with channel length. Here, the slope dR_{NW}/dL was found to be 790±31 kΩ/μm. The electronic mean free path λ_0 was estimated to be ~8.2 nm from the slope dR_{NW}/dL by $R_{NW}=(h/4e^2)L/\lambda_0$,[11,14] where h is Planck's constant and e is the electronic charge. The shortest channel length that could be made with our CAFM setup was 20 nm, suggesting that the transport is still in the diffusive regime.

Figure 3(a) shows the series source-drain current versus gate voltage (I_{DS}-V_G) at a fixed drain bias of 100 mV for different channel lengths. It can be seen that In_2O_3 nanowires behave like a n-type semiconductor, since the current increases with an increase in gate voltage. This n-type behavior of In_2O_3 can be attributed to oxygen vacancies acting as donors of electrons to the conduction band.[15] The inset in Fig. 3(a) shows the relationship between transconductance ($g_m=dI_{DS}/dV_G$) and channel length in the In_2O_3 nanowire FET at a zero gate bias. The g_m appears to increase gradually with decreasing channel length. The threshold voltage V_T was obtained from I_{DS}-V_G data for different channel lengths [Fig. 3(a)] and appears to shift with channel length, as shown in Fig. 3(b). As the channel length decreases, the threshold voltage V_T shifts from −3.2 V (1 μm channel length) to −5.5 V (20 nm channel length). This shift in threshold voltage indicates an increase in one-dimensional electron concentration (n) in the nanowire, estimated to range between 1.6×10^7 cm^{-1} (1 μm channel length) and 2.7×10^7 cm^{-1} (20 nm channel length), from $n=CV_T/eL$. Here, e is the electronic charge and $C=2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$ is the approximate capacitance of the nanowire, where ε is the dielectric constant of SiO_2 (3.9), h is the thickness of the SiO_2 layer (100 nm), and r is the radius of the In_2O_3 nanowire (12.5 nm).[16]

The V_T roll-off phenomenon [Fig. 3(b)] in the In_2O_3 nanowire device can be explained by the charge-sharing model in MOSFETs.[17] In this model, a significant portion of the charges is depleted by the source and drain junctions for short channel MOSFETs, such that the threshold voltage required to deplete the charges and create the on set of the

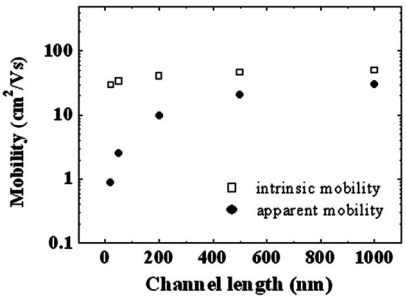

FIG. 4. Semilog plot of the measured apparent mobility (filled circles) and intrinsic mobility (open squares) values vs channel length. The intrinsic mobility values were obtained after correcting for parasitic contact resistance.

inversion layer decreases. In our case, the nanowire FET functions as an accumulation channel. Thus, because of the reduced effective nanowire channel length due to the non-negligible width of the Schottky barrier on the drain side for short channel nanowire FETs, it becomes easier to create an accumulation channel for a given gate bias. As a result, it was determined that V_T shifts in the negative gate bias direction as the channel length decreases. Though the drain-induced barrier lowering (DIBL) model is typically used to explain the threshold voltage V_T shift as a function of channel length and the drain bias, we did not perform V_{DS}-V_T characterization during our CAFM measurements in order to prevent potential damage to the CAFM tip and nanowire due to the high drain voltages applied for relatively elongated measurement time. However, in separate In_2O_3 nanowire FET devices with a fixed channel width of 3 μm, we observed V_T shift with drain voltage (not shown here). Consequently, we note that phenomenon a similar to the DIBL effect in conventional MOSFETs occurred in our In_2O_3 nanowire FET.

We also studied the scaling effect for the mobility of In_2O_3 nanowire FET as a function of channel length. It has been previously reported that parasitic contact resistance affects the evaluation of mobility values.[18] Thus, to extract the intrinsic mobility of the In_2O_3 nanowire FET, a correction for parasitic contact resistance is required.[19]

The parasitic contact resistance R_C at the source and drain contacts on the nanowire is assumed to be independent of L. R_{tot} can then be expressed as[18]

$$R_{tot}(L) = \left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{DS}\to 0} = R_{NW}(L) + R_C. \quad (1)$$

From Fig. 2(b), R_C was determined to be 500 ± 20 kΩ. The apparent mobility μ_a in the linear regime for the In_2O_3 nanowire FET was determined using Eq. (2),[20] and plotted as filled circles in Fig. 4(b).

$$\mu_a = \frac{L^2}{CV_{DS}}\frac{\partial I_{DS}}{\partial V_G}. \quad (2)$$

Subsequently, the intrinsic mobility μ_i values can be obtained after correction for R_C, as in Eq. (3),[19] and are plotted as open squares in Fig. 4(b).

$$\frac{\partial(\Delta R_{tot}/\Delta L)^{-1}}{\partial V_G} = \frac{\mu_i C}{L}. \quad (3)$$

From Fig. 4(b), it is clear that the apparent mobility values showed a larger reduction with decreasing channel length than the intrinsic mobility values. This is because, in shorter channel FETs, a relatively large fraction of the applied source-drain voltage drops over the parasitic contact resistance, as compared to long channel FETs. Although the intrinsic mobility values are corrected for R_C, there is a slight reduction in intrinsic mobility with decreasing channel length. It is known that increases in electron concentration lead to a reduction in mobility due to increased scattering.[20] As mentioned previously, in our In_2O_3 nanowire device the electron concentration increases with decreasing channel length. As a result, more electrons are able to accumulate within the nanowire channel as the channel length decreases, thus reducing its intrinsic mobility.

In conclusion, the channel-length dependence of the transfer characteristics of In_2O_3 nanowire field effect transistors was examined using conducting atomic force microscopy. It was determined that as the channel length decreased from 1 μm to 20 nm, a series of scaling effects was observed, i.e., the threshold voltage shifted in the negative gate bias direction, the source-drain current and transconductance increased, and the mobility decreased with a decreasing channel length. Additionally, as compared with the apparent mobility, the intrinsic mobility corrected for parasitic contact resistance was scaled less sensitively with respect to the channel length.

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